

Appl. No. 09/847,835  
Amendment Date: January 11, 2005  
Reply to Office Action of October 28, 2004

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application (it should be noted that claims cancelled are cancelled without prejudice):

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**LISTING OF THE CLAIMS**

Claim 1 (currently amended): A method for characterizing an electronic circuit comprising:

- 10 receiving design information from a circuit design tool;  
identifying an electrical circuit condition including one or more of a noise event, a  
coupling event, a race event and a dynamic hazard ~~identifying an electrical~~  
~~circuit condition that requires test based on the design information;~~  
determining a design verification test;  
evaluating the effectiveness of the design verification test in exercising the  
15 electrical circuit condition; and  
determining a second design verification test and also evaluating the effectiveness  
of the second design verification test in exercising the electrical circuit  
condition when the first design verification test does not effectively exercise  
the electrical circuit condition.

- 20 Claim 2 (original): The method of Claim 1 wherein determining a design  
verification test comprises:  
generating a design verification test using one or more of a manual test definition  
process, an algorithmic test definition process, a random test definition  
process and an exhaustive test definition process.

- 25 Claim 3 (original): The method of Claim 1 wherein evaluating the effectiveness  
of the design verification test comprises:  
executing the design verification test in a simulator; and  
recognizing the presence of the electrical circuit condition in the simulator results.

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Claim 4 (original): The method of Claim 1 wherein evaluating the effectiveness of the design verification test comprises:

representing the electrical condition in a simulator monitor function;  
executing the design verification test and the simulator monitor function in a  
5 simulator; and  
monitoring the activity of the simulator monitor function.

Claim 5 (original): The method of Claim 1 wherein receiving design information comprises:

parsing an output report from a circuit design tool; and  
10 generating tokens representing the parsed output report.

Claim 6 (cancelled).

Claim 7 (original): The method of Claim 1 wherein identifying an electrical circuit condition comprises:

receiving tokens descriptive of the design information; and  
15 analyze the structure of the tokens in accordance with a pre-established electrical event definition.

Claim 8 (original): The method of Claim 1 wherein evaluating the effectiveness of the design verification test comprises:

generating a description file readable by one or more of an automatic test pattern  
20 generator, a fault simulator, and a vector tester; and  
causing one or more of an automatic test pattern generator, a fault simulator, and a vector tester to be executed using said generated description file as an input.

Claim 9 (original): The method of Claim 1 further comprising:

receiving the electrical circuit condition in a design verification tool; and  
25 verifying the design of the electronic circuit based on the electrical circuit condition.

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Claim 10 (original): The method of Claim 9 wherein verifying the design comprises simulating one or more of a noise event, a coupling event, a timing event, a race event, and a dynamic hazard.

5 Claim 11 (original): The method of Claim 9 wherein verifying the design comprises automatically generating a test pattern for testing one or more of a noise event, a coupling event, a timing event, a race event, and a dynamic hazard.

Claim 12 (currently amended): An apparatus for characterizing an electronic circuit comprising:  
design information receiver capable of receiving design information;  
10 circuit condition identifier capable of identifying an electrical circuit condition including one or more of a noise event, a coupling event, a race event and a dynamic hazard in the design information that requires test;  
design verification test selection unit capable of selecting a first design verification test; and  
15 evaluation unit capable of evaluating the effectiveness of the first selected design verification test in exercising the identified circuit condition and wherein the design verification test selection unit is capable of selecting a second design verification test when the evaluation unit determines that the first selected design verification test is ineffective in exercising the identified circuit  
20 condition and wherein the evaluation unit is capable of evaluating the effectiveness of the second selected design verification test.

Claim 13 (original): The apparatus of Claim 12 wherein the design verification test selection unit comprises one or more of a manual test definition module, an automated test definition module, a random test definition module, and an exhaustive  
25 test definition module.

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Claim 14 (original): The apparatus of Claim 12 wherein the evaluation unit comprises:

executive module that conveys the design verification test to a simulator; and  
analyzer module that receives results from the simulator and issues a signal when  
5 the electrical circuit condition is recognized in said simulator results.

Claim 15 (original): The apparatus of Claim 12 wherein the evaluation unit comprises:

simulator monitor function receiver capable of receiving a simulator monitor  
function;  
10 executive module that conveys the design verification test and the received  
simulator monitor function to a simulator; and  
analyzer module that issues a signal when the simulator monitor function is  
triggered.

Claim 16 (original): The apparatus of Claim 12 wherein the design information  
15 receiver comprises a lexical analyzer capable of generating tokens according to an  
output report received from a circuit design tool.

Claim 17 (cancelled).

Claim 18 (original): The apparatus of Claim 12 wherein the circuit condition  
identifier comprises a parser capable of analyzing the structure of received tokens in  
20 accordance with a pre-established electrical event definition.

Claim 19 (original): The apparatus of Claim 12 wherein the evaluation unit comprises:

description file generator capable of generating a description file that is readable  
by one or more of an automatic test pattern generator, a fault simulator, and a  
25 vector tester; and

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test executive module capable of starting one or more of an automatic test pattern generator, a fault simulator, and a vector tester using said generated description file as an input.

Claim 20 (original): The apparatus of Claim 12 further comprising a design verification director capable of:

5 directing the received electrical condition to a design verification tool;  
starting a design verification tool;  
receiving an output from the design verification tool; and  
issuing a signal when the identified electrical circuit condition is not detected in  
10 the received design verification tool output.

Claim 21 (currently amended): A computer-readable medium having computer-executable functions for characterizing an electronic circuit comprising:

receiving design information from a circuit design tool;  
identifying an electrical circuit condition including one or more of a noise event, a  
15 coupling event, a race event and a dynamic hazard that requires test based on  
the design information;  
determining a design verification test;  
evaluating the effectiveness of the design verification test in exercising the  
electrical circuit condition; and  
20 determining a second design verification test and also evaluating the effectiveness  
of the second design verification test in exercising the electrical circuit  
condition when the first design verification test does not effectively exercise  
the electrical circuit condition.

Claim 22 (original): The computer-readable medium of Claim 21 wherein  
25 determining a design verification test comprises:  
generating a design verification test using one or more of a manual test definition  
process, an algorithmic test definition process, a random test definition  
process and an exhaustive test definition process.

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Claim 23 (original): The computer-readable medium of Claim 21 wherein  
evaluating the effectiveness of the design verification test comprises:  
executing the design verification test in a simulator; and  
recognizing the presence of the electrical circuit condition in the simulator results.

5 Claim 24 (original): The computer-readable medium of Claim 21 wherein  
evaluating the effectiveness of the design verification test comprises:  
representing the electrical condition in a simulator monitor function,  
executing the design verification test and the simulator monitor function in a  
simulator; and  
10 monitoring the activity of the simulator monitor function.

Claim 25 (original): The computer-readable medium of Claim 21 wherein  
receiving design information comprises:  
parsing an output report from a circuit design tool; and  
generating tokens representing the parsed output report.

15 Claim 26 (cancelled).

Claim 27 (original): The computer-readable medium of Claim 21 wherein  
identifying an electrical circuit condition comprises:  
receiving tokens descriptive of the design information; and  
analyze the structure of the tokens in accordance with a pre-established electrical  
20 event definition.

Claim 28 (original): The computer-readable medium of Claim 21 wherein  
evaluating the effectiveness of the design verification test comprises:  
generating a description file readable by one or more of an automatic test pattern  
generator, a fault simulator, and a vector tester; and  
25 causing one or more of an automatic test pattern generator, a fault simulator, and a  
vector tester to be executed using said generated description file as an input.

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Claim 29 (original): The computer-readable medium of Claim 21 further comprising:

receiving the electrical circuit condition in a design verification tool; and  
verifying the design of the electronic circuit based on the electrical circuit  
5 condition.

Claim 30 (original): The computer-readable medium of Claim 29 wherein  
verifying the design comprises simulating one or more of a noise event, a coupling  
event, a timing event, a race event, and a dynamic hazard.

Claim 31 (original): The computer-readable medium of Claim 29 wherein  
10 verifying the design comprises automatically generating a test pattern for testing one  
or more of a noise event, a coupling event, a timing event, a race event, and a  
dynamic hazard.

Claim 32 (currently amended): An apparatus for characterizing an electronic circuit  
comprising:

15 means for receiving circuit design information;  
means for identifying electrical circuit conditions including one or more of a noise  
event, a coupling event, a race event and a dynamic hazard that require test;  
means for selecting a first design verification test;  
means for evaluating the effectiveness of the first design verification test in  
20 exercising the identified electrical circuit condition; and  
means for selecting a second design verification test when the first design  
verification test is found to be ineffective.